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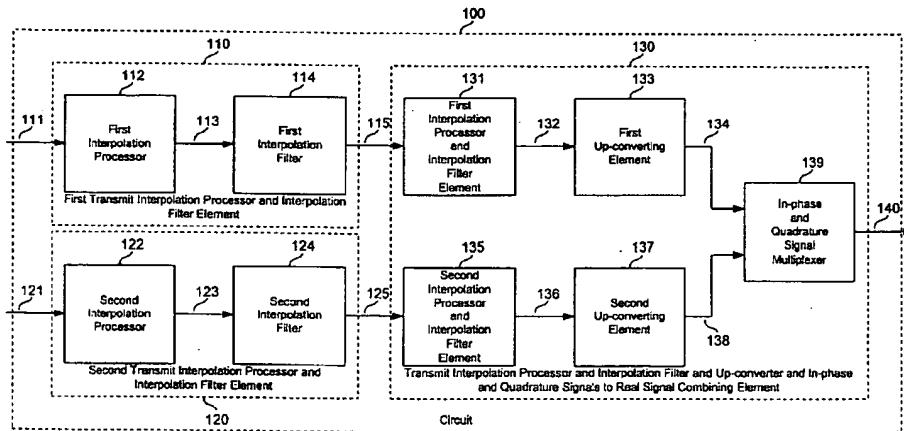
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(54) Title: DIGITAL CONVERSION BETWEEN COMPLEX BB SIGNALS AND REAL RF SIGNALS



(57) Abstract: A circuit and a method for converting base-band modulated in-phase and quadrature signals to an intermediate frequency centered real signal by: - dispersing spectra; - frequency up-shifting the dispersed spectra; and - mirroring the up-shifted dispersed spectra. The invention further relates to a circuit and a method for converting an intermediate frequency centered real signal to base-band modulated in-phase and quadrature signals by: - splitting spectra into real and imaginary parts; - frequency down-shifting the spectra; and - compressing the downshifted spectra. The invention further relates to an apparatus comprising the above-described circuits, and a computer readable medium hereto. The basic idea is to combine complex in-phase and quadrature signals into a real signal before the up-mixing process takes place in a transmitter by use of a signal combining circuit. Similar the basic idea is to split a real signal into complex in-phase and quadrature signals after the down-mixing process has taken place in a receiver by use of a signal splitting circuit.

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Digital conversion between complex BB signals and real RF signals

The present invention relates to a circuit and a method for converting base-band modulated in-phase and quadrature signals to an intermediate frequency centered real signal. The present invention further relates to a circuit and a method for converting an intermediate frequency centered real signal to base-band modulated in-phase and quadrature signals. The present invention further relates to an apparatus and a computer readable medium.

The field of use is complex signal receivers and complex signal transmitters, receiving or transmitting in-phase and quadrature signals, e.g. OFDM receivers and OFDM transmitters.

It is often desirable in communication systems to transmit a composite signal being a combination of two or more signals, combined by a predetermined method. The signals may represent voice communications, binary data communications, facsimile data, modem telecommunications, and similar signals. As an example, it is well known in the art to use time division multiplexing (or frequency division multiplexing) to generate a composite signal in which individual data signals are allocated a predetermined portion of the time (or the frequency spectrum) within the composite signal. Orthogonal frequency division multiplexing (OFDM) is a robust technique for efficiently transmitting information over a channel. The technique uses a plurality of sub-carrier frequencies (sub-carriers) within a channel to transmit the information. These sub-carriers are arranged for optimal channel efficiency compared to the more conventional transmission approaches, such as the frequency division multiplexing, which waste large portions of the channel in order to separate and isolate the sub-carrier frequency spectra and thereby avoid inter-carrier interference. The input signal to an OFDM transmitter and the output signal from an OFDM receiver are in the form of data bits. Besides of error detection and correction, OFDM features quadrature amplitude modulation encoding the data bits into complex-valued points, i.e. the OFDM transmitter output and the OFDM receiver input are complex signal data bits including real and imaginary parts.

In known cellular communication systems, the base band data is generally in digital format, often but not necessarily the result of a digital sampling of a voice or data

communication. Some prior art base stations convert the digital data signal to OFDM signals. Often conversion is done in a digital base band processor that modulates each digital modulating signal by the digital data signal and supplies each of the modulated signals to individual digital-to-analogue converters (DAC) and filters. Each of the individual analogue signals is then up converted to its assigned IF frequency and subsequently summed with the other channel (which have undergone the same process in parallel). The composite signal may then be modulated to the desired RF frequency for subsequent transmission. The prior art method requires separate DACs, smoothing filters, and up converters.

10

US patent 5,519,732 describes a system and method for converting and combining multiple digital base-band signals into a composite IF signal for subsequent up converting and transmitting as an RF signal. The system and method use distributed symmetrical circuit architecture to form a composite IF signal from multiple identical converting elements, which are daisy-chained together to produce the composite signal from the converted signals in each element. Circuit complexity is reduced by the use of the multiple identical elements each of which may be readily formed from a standard integrated circuit.

The circuit however requires two multipliers, one for the in-phase signal and 20 one for the quadrature signal.

It is therefore an object of the present invention to solve the above-mentioned problems.

25 This is, as achieved by a circuit comprising:

- means for dispersing spectra of the base band modulated in-phase and quadrature signals, the frequency difference between the dispersed spectra being at least twice the frequency difference of the spectra;
- means for up-shifting dispersed spectra of base band modulated in-phase and 30 quadrature signals, the shift up in frequencies of the dispersed spectra omitting at least zero frequency from the substantial part of the spectra; and
- means for mirroring up-shifted dispersed spectra of base band modulated in-phase and quadrature signals into a spectrum of the intermediate frequency centered real signal.

The terms "in-phase" and "quadrature signals" are used synonymously for complex signals having a real part and an imaginary part.

The term "spectrum" is used for the representation of a signal in the frequency domain, having spectral frequency components corresponding to the frequencies contained in the signal before the signal is sampled. The term spectrum is further used for each of the replicas of the spectrum in the frequency domain after the signal is sampled. For complex signals having an in-phase component and a quadrature component, the term spectrum is used for each of the replicas of the spectrum in the frequency domain corresponding to the frequencies included in the real part of the signal, and for each of the replicas of the spectrum in the frequency domain corresponding to the frequencies included in the imaginary part of the signal. When discussing Fig. 7, the term spectrum also refers to each of the replicas of the spectrum in the frequency domain corresponding to the frequencies included in the real part of the signal and to the frequencies included in the imaginary part of the signal merged together.

The term "frequency difference" is used to indicate a frequency range between an upper frequency limit and a lower frequency limit. As an example, a frequency difference of a spectrum is the frequency range comprising spectral frequency components of the spectrum, and a frequency difference between two spectra is the frequency range between the two spectra.

The term "dispersing" spectra is used when the difference in frequency between two consecutive replicas of the spectrum is enlarged as a result of an interpolation process and a filtering process.

The term "zero frequency" refers to the frequency component corresponding to DC.

The term "substantial part" of a spectrum refers to the necessary part of a spectrum required to restore the corresponding signal with an acceptable low distortion.

In an embodiment of the invention this is, as further disclosed in claim 11 achieved according to the invention by a circuit comprising:

- means for splitting a spectrum of the intermediate frequency centered real signal into spectra of intermediate frequency modulated in-phase and quadrature signals;
- means for down-shifting spectra of the intermediate frequency modulated in-phase and quadrature signals, the shift down in frequencies of the spectra inserting zero frequency into the center of the frequency difference of the spectra; and

- means for compressing down-shifted spectra of the intermediate frequency modulated in-phase and quadrature signals, the frequency difference between the compressed down-shifted spectra being at most half the frequency difference of the spectra;

The term "compressing" spectra is used when the difference in frequency 5 between two consecutive replicas of the spectrum is reduced as a result of a decimation process and a filtering process.

In a further embodiment this is, as further disclosed in claim 21 achieved according to the invention by a method comprising the steps of:

- dispersing spectra of the base band modulated in-phase and quadrature 10 signals, the frequency difference between the dispersed spectra being at least twice the frequency difference of the spectra;
- up-shifting dispersed spectra of base band modulated in-phase and quadrature signals, the shift up in frequencies of the dispersed spectra omitting at least zero frequency from the substantial part of the spectra;
- mirroring up-shifted dispersed spectra of base band modulated in-phase and quadrature signals into a spectrum of the intermediate frequency centered real signal; 15 and, as further disclosed in claim 31 achieved according to the invention by a method comprising the steps of:
 - splitting a spectrum of the intermediate frequency centered real signal into spectra of intermediate frequency modulated in-phase and quadrature signals; 20
 - down-shifting spectra of the intermediate frequency modulated in-phase and quadrature signals, the shift down in frequencies of the spectra inserting zero frequency into the center of the frequency difference of the spectra;
 - compressing down-shifted spectra of the intermediate frequency modulated 25 in-phase and quadrature signals, the frequency difference between the compressed down-shifted spectra being at most half the frequency difference of the spectra;
 - and, as further disclosed in claim 41 achieved according to the invention by an apparatus comprising a first circuit for performing any of the methods defined in claims 1 through 10 and a second circuit for performing any of the methods defined in claims 11 30 through 20,
 - and, as further disclosed in claim 42 achieved according to the invention by a computer readable medium having stored thereon instructions for determining one or more processing units to execute the methods according to any of the claims 21 through 30,

- and, as further disclosed in claim 43 achieved according to the invention by a computer readable medium having stored thereon instructions for determining one or more processing units to execute the methods according to any of the claims 31 through 40.

Hereby it is insured that the multipliers can be omitted, and that the transmitter 5 up-conversion and the receiver down-conversion are performed as multiplexing between the true and the negated value of the in-phase and quadrature signals. Also the filters of the invention have are relatively more efficient implemented resulting a simplified circuit layout and relatively low power consumption. When implementing a signal combining circuit in a transmitter, only one digital-to-analogue converter (DAC) is required. Similar, when 10 implementing a signal splitting circuit in a receiver, only one analogue-to-digital converter (ADC) is required. The transmitter and the receiver need only one analogue mixer. AC coupling is allowed for solving the problem of DC offset, since there is no information at DC frequency before the ADC. Also the transmitter and the receiver analogue filters are practically easier to be implemented, i.e. the filters can be implemented at a relatively low 15 cost.

The basic idea is to combine complex in-phase and quadrature signals into a real signal before the up-mixing process takes place in a transmitter by using a signal combining circuit, and to split a real signal into complex in-phase and quadrature signals after the down-mixing process has taken place in a receiver using a signal splitting circuit.

20 An interpolation process is considered a process in which the spectrum of a signal is dispersed by inserting one or more zero signal values between each discrete signal value. A discrete signal interpolated by one is unchanged. Interpolating by two means that one zero signal value is inserted between each discrete signal value. Interpolating by four means that the process is repeated twice, i.e. a total of three zero signal values are inserted 25 between each discrete signal value.

A decimation process is considered a process in which the spectrum of a signal is compressed i.e. the decimation process is a reverse process to the interpolation process.

30 A poly phase implementation of an interpolate by two half band filter is considered a circuit similar to the circuit shown in HSP43216 data sheet from Intersil, September 2000, File Number 3365.8, page 3-10, Fig. 10.

A poly phase implementation of a quadrature to real converter is considered to be a circuit similar to the circuit in HSP43216 data sheet from Intersil, September 2000, File Number 3365.8, page 3-14, Fig. 20.

A poly phase implementation of a decimate by two half band filter is considered a circuit similar to the circuit in HSP43216 data sheet from Intersil, September 2000, File Number 3365.8, page 3-8, Fig. 6.

5 A poly phase implementation of a real to quadrature converter is considered a circuit similar to the circuit in HSP43216 data sheet from Intersil, September 2000, File Number 3365.8, page 3-12, Fig. 14.

An embodiment of the circuit as disclosed in claim 2 has the advantage that the interpolation number can be selected in accordance with the requirements for dispersing the spectra, i.e. the required dispersing of the spectra in order to be able (after up-conversion) 10 to mirror the dispersed spectra without overlapping any spectral components. In addition, the filters will omit any unwanted spectral components from the dispersed spectra. The process of filtering can be performed in one or two steps using the first interpolation filter and the second interpolation filter, and/or using the third interpolation filter and the fourth interpolation filter. It is therefore possible to select filters from an extended range of filter 15 characteristics, i.e. from simple filter characteristics requiring a one step filtering, to more complicated filter characteristics requiring two step filtering. Similarly, the process of interpolation can be performed in one or two steps using the first interpolation processor and the second interpolation processor, and/or using the third interpolation processor and the fourth interpolation processor. It is therefore possible to optimize the circuit as a trade-off 20 between the necessary interpolation and the necessary filtering against circuit complexity.

An embodiment of the circuit as disclosed in claim 3 has the advantage that the dispersed spectra can be shifted up in frequency, in order to omit the zero frequency from the spectra. This makes it possible to mirror the dispersed spectra without overlapping any spectral components. Also any zero frequency (DC component) is not lost during a 25 subsequent aerial transmission, as the zero frequency is frequency up-shifted too.

An embodiment of the circuit as disclosed in claim 4 has the advantage that the up-converted dispersed spectra are converted to real spectra. This makes possible the transmission of the spectra without distortion that could result from loss of imaginary spectral components.

30 An embodiment of the circuit as disclosed in claim 5 has the advantage that the filtered spectrum may be in the range from zero frequency (DC) and up to a maximal frequency. Therefore, the circuit (and then the transmitter) is able to transmit low pass filtered signals, e.g. a high fidelity voice signal.

An embodiment of the circuit as disclosed in claim 6 has the advantage that the implementation of the filters are greatly simplified, as half of the filter coefficients are zero.

Using the circuits disclosed in claims 7, 8 and 9 has the advantage that the 5 spectra of an OFDM signal may be transmitted, an OFDM signal may be transmitted with minimal distortion and the circuit for an OFDM signal is implemented with minimal circuit complexity, respectively.

An embodiment of the circuit as disclosed in claim 10 has the advantage that up-conversion is performed by means of simple +/-1 multiplications, reducing the circuit 10 complexity. No multipliers are therefore required.

An embodiment of the circuit as disclosed in claim 12 has the advantage that the real spectra can be processed as complex spectra after de-multiplexing. This makes possible a restoration of the complex spectra having relatively low distortion, the distortion resulting from loss of imaginary spectral components.

15 An embodiment of the circuit as disclosed in claim 13 has the advantage that the spectra can be shifted down in frequency, inserting the zero frequency into the center of the frequency difference of the spectra. The spectra will therefore be equivalent to the dispersed (but not up-converted) spectra of the transmitting circuit. This makes possible the restoration of the spectra that are dispersed by the transmitter.

20 An embodiment of the circuit as disclosed in claim 14 has the advantage that the decimation number can be selected in accordance with the requirements for compressing the spectra, i.e. the required compressing for restoring the original transmitted spectra being transmitted. In addition, the filters will omit any unwanted spectral components from the compressed spectra restoring the complex spectra. The process of filtering can be performed 25 in one or two steps using the first decimation filter and the second decimation filter, and/or using of the third decimation filter and the fourth decimation filter. It is therefore possible to select filters having different characteristics, i.e. from simple filter performing filtering in one step, to more complicated filters performing filtering over two steps. Similarly, the process of decimation can be performed in one or two steps using the first decimation processor and the 30 second decimation processor, and/or using the third decimation processor and the fourth decimation processor. It is therefore possible to optimize the circuit as a trade-off between the necessary decimation and the necessary filtering against circuit complexity, similar to for the transmitting circuit.

An embodiment of the circuit as disclosed in claim 15 has the advantage that the filtered spectrum may be in the range from zero frequency (DC) and up to a maximal frequency. The circuit (and then the receiver) is therefore capable to receive low pass filtered signals with requirements to the lower frequencies, e.g. a high fidelity voice signal.

5 An embodiment of the circuit as disclosed in claim 16 has the advantage that the implementation of the filters are greatly simplified, as half of the filter coefficients are zero.

An embodiment of the circuit as disclosed in claim 17 has the advantage that the spectra of an OFDM signal may be received using the circuit.

10 An embodiment of the circuit as disclosed in claim 18 has the advantage that an OFDM signal may be received using the circuit, and with minimal distortion.

An embodiment of the circuit as disclosed in claim 19 has the advantage that the circuit for an OFDM signal is implemented with minimal circuit complexity.

15 An embodiment of the circuit as disclosed in claim 20 has the advantage that down-conversion is performed by means of +/-1 multiplications, reducing the circuit complexity. No multipliers are therefore required.

The embodiments of the methods as disclosed in claims 22 through 30 has the same advantages as the embodiments of the circuits as disclosed in claims 2 through 10.

20 The embodiments of the methods as disclosed in claims 32 through 40 has the same advantages as the embodiments of the circuits as disclosed in claims 12 through 20.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

25 In the following embodiments of the invention will be described referring to the figures, wherein

Fig. 1 depicts an embodiment of an in-phase and quadrature signals to real signal combining circuit according to the invention, and

30 Fig. 2 depicts an embodiment of an interpolation process element and a filter element according to the invention, and

Fig. 3 depicts an embodiment of an interpolation process element and a filter element and an up-converter and an in-phase and quadrature signals to real signal combining element according to the invention, and

Fig. 4 depicts an embodiment of a real signal to in-phase and quadrature signals splitting circuit according to the invention, and

Fig. 5 depicts an embodiment of a decimation process element and a filter element according to the invention, and

5 Fig. 6 depicts an embodiment of a decimation process element and a filter element and a down-converter and a real signal to in-phase and quadrature signals splitting element according to the invention, and

Fig. 7 depicts signal spectrums at various locations on a signal combining circuit and a signal splitting circuit.

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Fig. 1 depicts circuit 100 for combining an in-phase signal and a quadrature signal according to the invention. An in-phase branch 111 of in-phase and quadrature signals is an input to a first interpolation processor 112. An interpolated in-phase branch 113 of in-phase and quadrature signals is an output from the first interpolation processor 112 and an input to a first interpolation filter 114. A filtered interpolated in-phase branch 115 of in-phase and quadrature signals is an output from the first interpolation filter 114 and an input to a first interpolation processor and interpolation filter element 131. The first interpolation processor 112 and the first interpolation filter 114 forms a first transmit interpolation processor and interpolation filter element 110. A quadrature branch 121 of in-phase and quadrature signals is an input to a second interpolation processor 122. An interpolated quadrature branch 123 of in-phase and quadrature signals is an output from the second interpolation processor 122 and an input to a second interpolation filter 124. A filtered interpolated quadrature branch 125 of in-phase and quadrature signals is an output from the second interpolation filter 124 and an input to a second interpolation processor and interpolation filter element 135. The second interpolation processor 122 and the second interpolation filter 124 forms a second transmit interpolation processor and interpolation filter element 120. A double filtered double interpolated in-phase branch 132 of in-phase and quadrature signals is an output from the first interpolation processor and interpolation filter element 131 and an input to a first up-converting element 133. An up-converted double filtered double interpolated in-phase branch 134 of in-phase and quadrature signals is an output from the first up-converting element 133 and a first input to an in-phase and quadrature signal multiplexer 139. A double filtered double interpolated quadrature branch 136 of in-phase and quadrature signals is an output from the second interpolation processor and interpolation filter element 135 and an input to a

second up-converting element 137. An up-converted double filtered double interpolated quadrature branch 138 of in-phase and quadrature signals is an output from the second up-converting element 137 and a second input to the in-phase and quadrature signal multiplexer 139. A real signal 140 is an output from the in-phase and quadrature signal multiplexer 139.

5 The first interpolation processor and interpolation filter element 131 and the first up-converting element 133 and the second interpolation processor and interpolation filter element 135 and the second up-converting element 137 and the in-phase and quadrature signal multiplexer 139 forms a transmit interpolation processor and interpolation filter and up-converter and in-phase and quadrature signals to real signal combining element 130.

10 The first interpolation processor 112 inserts a zero signal value between each discrete signal value of the in-phase branch of in-phase and quadrature signals 111. Similar the second interpolation processor 122 inserts a zero signal value between each discrete signal value of the quadrature branch of in-phase and quadrature signals 121. These processes spreads the spectral components of the in-phase and quadrature signals from repeating

15 themselves with a frequency difference of the sampling frequency to repeating themselves with a frequency difference of the double of the sampling frequency. The first interpolation filter 114 filters the interpolated in-phase branch of in-phase and quadrature signals 113. Similar the second interpolation filter 124 filters the interpolated quadrature branch of in-phase and quadrature signals 123. The filtering is performed using half-band filters. A half-

20 band filter utilizes a symmetrical filter characteristic where half of the coefficients are equal to zero. Consequently the implementation of the interpolation processors 112, 122 and interpolation filters 114, 124 can be simplified, as further detailed in Fig. 2. It should however be noted that other filter characteristics may be applicable for other applications, and the invention is by no means limited to utilizing half-band filters. Also the number of

25 filter coefficients may vary from application to application. The first interpolation processor and filter element 131 and the second interpolation processor and filter element 135 are basically performing similar operations as of the first interpolation processor 112 and the first interpolation filter 114, and of the second interpolation processor 122 and the second interpolation filter 124 respectively. As the filter requirements for the interpolation filters

30 131, 135 practically are easier to implement than for the first interpolation filter 114 and for the second interpolation filter 124, the filters are typically implemented with less filter coefficients. A zero signal value is inserted between each discrete signal value on the filtered interpolated in-phase and quadrature signals 115, 125. These processes spreads the spectral components of the filtered interpolated in-phase and quadrature signals 115, 125 from

repeating themselves with a frequency difference of twice the sampling frequency to repeating themselves with a frequency difference of the fourth of the sampling frequency. Again filtering is performed using half-band filters. The implementation of the interpolation processors 131, 135 and interpolation filters 131, 135 are simplified, as further detailed in

5 Fig. 3. It should however be noted that other filter characteristics may be applicable for other applications, and the invention is by no means limited to utilizing half-band filters. Also the number of filter coefficients may vary from application to application. The first up-converting element 133 converts the spectral components of the double filtered double interpolated in-phase branch of in-phase and quadrature signals 132 up in frequency by an

10 amount equal to the sampling frequency. Similar the second up-converting element 137 converts the spectral components of the double filtered double interpolated quadrature branch of in-phase and quadrature signals 136 up in frequency by an amount equal to the sampling frequency. The in-phase and quadrature signal multiplexer 139 finally multiplexes the up-converted double filtered double interpolated in-phase branch of in-phase and quadrature

15 signals 134 and the up-converted double filtered double interpolated quadrature branch of in-phase and quadrature signals 138 to form the real signal 140. By multiplexing the up-converted double filtered double interpolated in-phase and quadrature signals 134, 138, the corresponding spectral components of the signals are mirrored round the zero frequency resulting in a real signal 140.

20 Fig. 2 depicts element 210 for interpolating and filtering an in-phase signal or a quadrature signal according to the invention. 250 is an adding element. 251 is a discrete filter signal. 252 is a multiplying element. 253 is a latching element. 254 is a multiplexing element. A branch 211 of in-phase and quadrature signals is an input to a series of cascade coupled latching elements 260 and an input to a first delay 263. An output from the first

25 delay 263 is connected to an input on a second delay 264. Seven pairs of outputs from the series of cascade coupled latching elements 260 is connected to seven pairs of inputs on a group of adders in series with multipliers 261. Seven outputs from the group of adders in series with multipliers 261 is connected to seven inputs on an expanded adder 262. An output from the expanded adder 262 is connected to a first input on a signal multiplexer 265. An

30 output from the second delay 264 is connected to a second input on the signal multiplexer 265. A filtered interpolated branch 215 of in-phase and quadrature signals is an output from the signal multiplexer 265.

If a half-band filter is implemented with 29 coefficients (labeled h_0 through h_{28}), the half-band filter utilize a characteristic with all even coefficients equal to zero except

for coefficient h_{14} which has a value of approximately 1. As the half-band filter for the odd coefficients utilize symmetrical characteristics, the implementation of the filter can be made very simple as illustrated on Fig. 2. In this implementation the input signal 211 is fed to a series of cascade coupled latching elements 260. The series of cascade coupled latching elements 260 includes only latching elements 253 using nonzero discrete filter signals 251, i.e. discrete filter signals corresponding to nonzero filter coefficients. Filtering is performed, by folding the input signal with the discrete filter signals. The folding process involves calculating each current discrete output as the sum of the current discrete input and the fourteen earlier discrete inputs, each discrete input weighted by the discrete filter signals. As the half-band filter is utilizing a symmetrical filter characteristic, the discrete input values in the series of cascade coupled latching elements 260 can be added two by two before multiplying by the corresponding discrete filter signal. The weighted values are then added all together in the expanded adder 262. Since the coefficient h_{14} is approximately 1, the implementation for this contribution to the folding process turns out to be a delay (the first delay 263). The second delay 264 is implemented in order to synchronize the contribution from the discrete filter signal corresponding to filter coefficient h_{14} to the contributions from the discrete filter signals corresponding to the odd filter coefficients. The contribution from the discrete filter signals corresponding to filter coefficient h_{14} is then multiplexed by the contributions from the discrete filter signals corresponding to the odd filter coefficients at the multiplexing element 254 as part of the interpolation process. The process may however be simplified, as described in the HSP43216 data sheet from Intersil, September 2000, File Number 3365.8, page 3-10, Fig. 9 and Fig. 10.

Fig. 3 depicts element 330 for interpolating and filtering and up converting and combining an in-phase signal and a quadrature signal according to the invention. 350 is an adding element. 351 is a discrete filter signal. 352 is a multiplying element. 353 is a latching element. 354 is a multiplexing element. 355 is an inverting element. 356 is a one-bit counter with a true output and a negated output. An in-phase branch 315 of in-phase and quadrature signals is an input to a series of cascade coupled latching elements 360. Three pairs of outputs from the series of cascade coupled latching elements 360 is connected to three pairs of inputs on a group of adders in series with multipliers 361. Three outputs from the group of adders in series with multipliers 361 is connected to three inputs on an expanded adder 362. A quadrature branch 325 of in-phase and quadrature signals is an input to a first delay 363. An output from the first delay 363 is connected to an input on a second delay 364. An output from the expanded adder 362 is connected to a first input on a complex signal up-

converter 366. An output from the second delay 364 is connected to a second input on the complex signal up-converter 366. A first output from the complex signal up-converter 366 is connected to a first input on a signal multiplexer 365. A second output from the complex signal up-converter 366 is connected to a second input on the signal multiplexer 365. A real signal 340 is an output from the signal multiplexer 365.

The interpolation process and filtering is performed in a similar way as described for Fig. 2. Up-conversion includes multiplying the real part of the signal with the cosine wave clock frequency, and multiplying the imaginary part of the signal with the sine wave clock frequency. By performing the process discrete, the cosine wave multiplication becomes equal to multiplying in turn with 0, 1, 0, -1... etc. Similar the sine wave multiplication becomes equal to multiplying in turn with -1, 0, 1, 0... etc. Adding the up-converted real part of the signal and the up-converted imaginary part of the signal yields a resulting real signal with mirrored spectral components. The process may however be simplified, as described in the HSP43216 data sheet from Intersil, September 2000, File Number 3365.8, page 3-14, Fig. 19 and Fig. 20. In accordance with the data sheet, the above-described process can be implemented by feeding the real part of a signal to the even coefficients of a half-band filter, and feeding the imaginary part of the same signal to the odd coefficients of the half-band filter. The up-conversion is then reduced to multiplying the real part of the signal in turn with 1, -1... etc. and multiplying the imaginary part of the signal in turn with -1, 1... etc. Multiplexing the up-converted real part of the signal and the up-converted imaginary part of the signal yields a resulting real signal with mirrored spectral components.

Fig. 4 depicts circuit 400 for splitting a real signal according to the invention. A real signal 440 is an input to an in-phase and quadrature signal de-multiplexer 439. An in-phase branch 434 of in-phase and quadrature signals is a first output from the in-phase and quadrature signal de-multiplexer 439 and an input to a first down-converting element 433. A down-converted in-phase branch 432 of in-phase and quadrature signals is an output from the first down-converting element 433 and an input to a first decimation processor and decimation filter element 431. A filtered decimated down-converted in-phase branch 415 of in-phase and quadrature signals is an output from the first decimation processor and decimation filter element 431 and an input to a first decimation processor 414. A quadrature branch 438 of in-phase and quadrature signals is a second output from the in-phase and quadrature signal de-multiplexer 439 and an input to a second down-converting element 437. A down-converted quadrature branch 436 of in-phase and quadrature signals is an output

from the second down-converting element 437 and an input to a second decimation processor and decimation filter element 435. A filtered decimated down-converted quadrature branch 425 of in-phase and quadrature signals is an output from the second decimation processor and decimation filter element 435 and an input to a second decimation processor 424. The in-

5 phase and quadrature signal de-multiplexer 439 and the first down-converting element 433 and the first decimation processor and decimation filter element 431 and the second down-converting element 437 and the second decimation processor and decimation filter element 435 forms a receive decimation processor and decimation filter and down-converter and real signal to in-phase and quadrature signals splitting element 430. A filtered double decimated

10 down-converted in-phase branch 413 of in-phase and quadrature signals is an output from the first decimation processor 414 and an input to a first decimation filter 412. A double filtered double decimated down-converted in-phase branch 411 of in-phase and quadrature signals is an output from the first decimation filter 412. The first decimation processor 414 and the first decimation filter 412 forms a first receive decimation processor and decimation filter element

15 410. A filtered double decimated down-converted quadrature branch 423 of in-phase and quadrature signals is an output from the second decimation processor 424 and an input to a second decimation filter 422. A double filtered double decimated down-converted quadrature branch 421 of in-phase and quadrature signals is an output from the second decimation filter 422. The second decimation processor 424 and the second decimation filter 422 forms a

20 second receive decimation processor and decimation filter element 420.

Basically the real signal to in-phase and quadrature signals splitting circuit 400 performs the reverse operation of the in-phase and quadrature signals to real signal combining circuit 100 of Fig. 1. The steps involve:

- splitting the real signal 440 into an in-phase branch of in-phase and
- 25 quadrature signals 434 and a quadrature branch of in-phase and quadrature signals 438 by use of an in-phase and quadrature signal de-multiplexer 439,
- down-converting the in-phase branch of in-phase and quadrature signals 434 by use of the first down-converting element 433, and down-convert the quadrature branch of in-phase and quadrature signals 438 by use of the second down-converting element 437,
- 30 - decimate and filter the down-converted in-phase branch of in-phase and quadrature signals 432 by use of the first decimation processor and filter element 431, and decimate and filter the down-converted quadrature branch of in-phase and quadrature signals 436 by use of the second decimation processor and filter element 435,

- decimate and filter the filtered decimated down-converted in-phase branch of in-phase and quadrature signals 415 by use of the first decimation processor 414 and the first decimation filter 412, and decimate and filter the filtered decimated down-converted quadrature branch of in-phase and quadrature signals 425 by use of the second decimation processor 424 and the second decimation filter 422.

Fig. 5 depicts element 510 for decimating and filtering an in-phase signal or a quadrature signal according to the invention. 550 is an adding element. 551 is a discrete filter signal. 552 is a multiplying element. 553 is a latching element. 554 is a de-multiplexing element. A branch 515 of in-phase and quadrature signals is an input to a signal de-multiplexer 565. A first output from the signal de-multiplexer 565 is connected to an input on a series of cascade coupled latching elements 560. Seven pairs of outputs from the series of cascade coupled latching elements 560 is connected to seven pairs of inputs on a group of adders in series with multipliers 561. Seven outputs from the group of adders in series with multipliers 561 is connected to seven inputs on an expanded adder 562. An output from the expanded adder 562 is connected to a first input on a signal adder 567. A second output from the signal de-multiplexer 565 is connected to an input on a first delay 563. An output from the first delay 563 is connected to an input on a second delay 564. An output from the second delay 564 is connected to a second input on the signal adder 567. A filtered decimated branch 511 of in-phase and quadrature signals is an output from the signal adder 567.

If a half-band filter is implemented similar to the filter on Fig. 2 with 29 coefficients (labeled h0 through h28), the half-band filter utilize a characteristic with all even coefficients equal to zero except for coefficient h14 which has a value of approximately 1. As the half-band filter for the odd coefficients utilize symmetrical characteristics, the implementation of the filter can be made very simple as illustrated on Fig. 5. In this implementation the input signal 515 is fed to a de-multiplexing element 554 as part of the decimation process. The de-multiplexed signal is fed to a series of cascade coupled latching elements 560 including only latching elements 553 using nonzero discrete filter signals 551, i.e. discrete filter signals corresponding to nonzero filter coefficients. Filtering is performed, by folding the input signal with the discrete filter signals. This involves calculating each current discrete output as the sum of the current discrete input and the fourteen earlier discrete inputs, each discrete input weighted by the discrete filter signals. As the half-band filter is utilizing a symmetrical filter characteristic, the discrete input values in the series of cascade coupled latching elements 560 can be added two by two before multiplying by the corresponding discrete filter signal. The weighted values are then added all together in the

expanded adder 562. Since the coefficient $h14$ is approximately 1, the implementation for this contribution to the folding process turns out to be a delay (the first delay 563). The second delay 564 is implemented in order to synchronize the contribution from the discrete filter signal corresponding to filter coefficient $h14$ to the contributions from the discrete filter signals corresponding to the odd filter coefficients. The contribution from the discrete filter signal corresponding to filter coefficient $h14$ is then added to the contributions from the discrete filter signals corresponding to the odd filter coefficients at the signal adder 567. The process may however be simplified, as described in the HSP43216 data sheet from Intersil, September 2000, File Number 3365.8, page 3-8, Fig. 5 and Fig. 6.

Fig. 6 depicts element 630 for decimating and filtering and down converting and splitting a real signal according to the invention. 650 is an adding element. 651 is a discrete filter signals. 652 is a multiplying element. 653 is a latching element. 654 is a de-multiplexing element. 655 is an inverting element. 656 is a one-bit counter with a true output and a negated output. A real signal 640 is an input to a signal de-multiplexer 665. A first output from the signal de-multiplexer 665 is connected to a first input on a complex signal down-converter 666. A second output from the signal de-multiplexer 665 is connected to a second input on the complex signal down-converter 666. A first output from the complex signal down-converter 666 is connected to a series of cascade coupled latching elements 660. Three pairs of outputs from the series of cascade coupled latching elements 660 is connected to three pairs of inputs on a group of adders in series with multipliers 661. Three outputs from the group of adders in series with multipliers 661 is connected to three inputs on an expanded adder 662. A filtered decimated down-converted in-phase branch 615 of in-phase and quadrature signals is an output from the expanded adder 662. A second output from the complex signal down-converter 666 is connected to an input on a first delay 663. An output from the first delay 663 is connected to an input on a second delay 664. A filtered decimated down-converted quadrature branch 625 of in-phase and quadrature signals is an output from the second delay 664.

The real input signal 640 is de-multiplexed by the de-multiplexing element 654 into a complex signal. The complex signal is then down-converted. Down-conversion includes multiplying the real part of the signal with the cosine wave clock frequency, and multiplying the imaginary part of the signal with the sine wave clock frequency. By performing the process discrete, the cosine wave multiplication becomes equal to multiplying in turn with 0, 1, 0, -1... etc. Similar the sine wave multiplication becomes equal to multiplying in turn with -1, 0, 1, 0... etc. The decimation process and filtering is performed

in similar ways as described for Fig. 5. The process may however be simplified, as described in the HSP43216 data sheet from Intersil, September 2000, File Number 3365.8, page 3-12, Fig. 13 and Fig. 14. In accordance with the data sheet, the down-conversion is then reduced to multiplying the real part of the signal in turn with 1, -1... etc. and multiplying the 5 imaginary part of the signal in turn with -1, 1... etc., and the decimation process and the filtering can be implemented by feeding the real part of a signal to the even coefficients of a half-band filter, and feeding the imaginary part of the same signal to the odd coefficients of the half-band filter.

Fig. 7 depicts signal spectrum at various locations on a signal combining 10 circuit and a signal splitting circuit. 770 is a spectrum of in-phase and quadrature signals. 771 is a spectrum of converted in-phase and quadrature signals. 776 is a spectrum of twice converted in-phase and quadrature signals. 777 is a spectrum of three times converted in-phase and quadrature signals. 772 is a spectrum of a real signal. 773 is a frequency axis. 774 is an amplitude axis. 775 is a sampling frequency B. 778 is a frequency difference between 15 spectra.

The spectrum of the in-phase an quadrature signals 770 represents the spectrum of the complex input signals 111, 121 to the in-phase and quadrature signals to real signal combining circuit 100 on Fig. 1. The spectrum of the in-phase an quadrature signals 770 also represents the spectrum of the complex output signals 411, 421 from the real signal 20 to in-phase and quadrature signals splitting circuit 400 on Fig. 4. Due to sampling, the spectrum 770 is repeated by multiples of the sampling frequency 775. Since the signal is complex the property of spectrum will not be symmetrical. 771 represents the spectrum of the filtered interpolated in-phase and quadrature signals 115, 125 of the in-phase and quadrature signals to real signal combining circuit 100 on Fig. 1. 771 also represents the spectrum of the 25 filtered decimated down-converted in-phase and quadrature signals 415, 425 of the real signal to in-phase and quadrature signals splitting circuit 400 on Fig. 4. Due to the interpolation process and filtering by the elements 110, 120, the spectrum is repeated by multiples of the sampling frequency 775 times two. Since the signal is complex the property of spectrum will not be symmetrical. 776 represents the spectrum of the double filtered 30 double interpolated in-phase and quadrature signals 132, 136 of the in-phase and quadrature signals to real signal combining circuit 100 on Fig. 1. 776 also represents the spectrum of the down-converted in-phase and quadrature signals 432, 436 of the real signal to in-phase and quadrature signals splitting circuit 400 on Fig. 4. Due to the interpolation process and filtering by the elements 110, 120, 131, 135 the spectrum is repeated by multiples of the

sampling frequency 775 times four. Since the signal is complex the property of spectrum will not be symmetrical. 777 represents the spectrum of the up-converted double filtered double interpolated in-phase and quadrature signals 134, 138 of the in-phase and quadrature signals to real signal combining circuit 100 on Fig. 1. 777 also represents the spectrum of the in-
5 phase and quadrature signals 434, 438 of the real signal to in-phase and quadrature signals splitting circuit 400 on Fig. 4. Due to the up-conversion by the elements 133, 137 the spectrum is shifted up in frequency by an amount equal to the sampling frequency 775. The element 139 multiplexes the complex signals 134, 138 in to the real signal 140 exhibiting a symmetrical (mirrored) spectrum 772. The real signal 440 is input to the real signal to in-
10 phase and quadrature signals splitting circuit 400 on Fig. 4.

It is remarked that the scope of protection of the invention is not restricted to the embodiments described herein. Neither is the scope of protection of the invention restricted by the reference numerals in the claims. The word 'comprising' does not exclude other parts than those mentioned in the claims. The word 'a(n)' preceding an element does
15 not exclude a plurality of those elements. Means forming part of the invention may both be implemented in the form of dedicated hardware or in the form of a programmed purpose processor. The invention resides in each new feature or combination of features.

CLAIMS:

1. A circuit (100) for converting base-band modulated in-phase and quadrature signals (111, 121) to an intermediate frequency centered real signal (140), characterized in that the circuit (100) comprises:
 - means for dispersing spectra of the base band modulated in-phase and quadrature signals (111, 121), the frequency difference between the dispersed spectra being at least twice the frequency difference of the spectra;
 - means for up-shifting dispersed spectra of base band modulated in-phase and quadrature signals (132, 136), the shift up in frequencies of the dispersed spectra omitting at least zero frequency from the substantial part of the spectra;
 - 10 - means for mirroring up-shifted dispersed spectra of base band modulated in-phase and quadrature signals (134, 138) into a spectrum of the intermediate frequency centered real signal (140).
2. A circuit (100) according to claim 1, wherein the means for dispersing spectra of the base band modulated in-phase and quadrature signals (111, 121) comprise:
 - a first interpolation processor (112) for interpolating an in-phase branch of the in-phase and quadrature signals (111) by at least one;
 - a second interpolation processor (122) for interpolating a quadrature branch of the in-phase and quadrature signals (121) by at least one;
 - 20 - a first interpolation filter (114) for filtering an interpolated in-phase branch of the in-phase and quadrature signals (113);
 - a second interpolation filter (124) for filtering an interpolated quadrature branch of the in-phase and quadrature signals (123);
 - a third interpolation processor (131) for interpolating a filtered interpolated in-phase branch of the in-phase and quadrature signals (115) by at least one;
 - 25 - a fourth interpolation processor (135) for interpolating a filtered interpolated quadrature branch of the in-phase and quadrature signals (125) by at least one;
 - a third interpolation filter (131) for filtering a filtered double interpolated in-phase branch of the in-phase and quadrature signals;

- a fourth interpolation filter (135) for filtering a filtered double interpolated quadrature branch of the in-phase and quadrature signals.

3. A circuit (100) according to claim 1 or 2, wherein the means for up-shifting dispersed spectra of the base band modulated in-phase and quadrature signals (132, 136) comprise:

- a first up-converting element (133) for frequency up-converting a double filtered double interpolated in-phase branch of the in-phase and quadrature signals (132);
- a second up-converting element (137) for frequency up converting a double filtered double interpolated quadrature branch of the in-phase and quadrature signals (136).

4. A circuit (100) according to at least one of the claims 1 to 3, wherein the means for mirroring up-shifted dispersed spectra of the base band modulated in-phase and quadrature signals (134, 138) comprises a multiplexer (139) for multiplexing an up-converted double filtered double interpolated in-phase branch of the in-phase and quadrature signals (134) and an up-converted double filtered double interpolated quadrature branch of the in-phase and quadrature signals (138) to a real signal (140).

5. A circuit (100) according to at least one of the claims 2 to 4, wherein at least one of the interpolation filters (114, 124, 131, 135) is a low pass filter.

6. A circuit (100) according to claim 5, wherein at least one of the low pass filters (114, 124, 131, 135) is a half band filter.

25 7. A circuit (100) according to at least one of the claims 2 to 6, wherein the circuit (100) is adapted for interpolating the in-phase and quadrature signals (111, 121) by four.

8. A circuit (100) according to claim 7, wherein

30 - the first interpolation processor (112) is adapted for interpolating the in-phase branch of the in-phase and quadrature signals (111) by two;

- the second interpolation processor (122) is adapted for interpolating the quadrature branch of the in-phase and quadrature signals (121) by two;

- the third interpolation processor (131) is adapted for interpolating the filtered interpolated in-phase branch of the in-phase and quadrature signals (115) by two;

- the fourth interpolation processor (135) is adapted for interpolating the filtered interpolated quadrature branch of the in-phase and quadrature signals (125) by two.

5

9. A circuit (100) according to at least one of the claims 2 to 8, wherein

- the first interpolation processor (112) and the first interpolation filter (114) is a poly phase implementation of an interpolate by two half band filter;

10 10 (124) is a poly phase implementation of an interpolate by two half band filter;

- the third interpolation processor (131) and the third interpolation filter (131) and the first up-converting element (133) and the fourth interpolation processor (135) and the fourth interpolation filter (135) and the second up-converting element (137) and the multiplexer (139) is a poly phase implementation of a quadrature to real converter.

15

10. A circuit (100) according to claim 9, wherein

- the first up-converting element (133) is implemented as a multiplexer adapted for multiplexing between a true and a negated value of the double filtered double interpolated in-phase branch of the in-phase and quadrature signals (132);

20 - the second up-converting element (137) is implemented as a multiplexer adapted for multiplexing between a true and a negated value of the double filtered double interpolated quadrature branch of the in-phase and quadrature signals (136).

11. A circuit (400) for converting an intermediate frequency centered real signal (440) to base-band modulated in-phase and quadrature signals (411, 421), characterized in 25 that the circuit (400) comprises:

- means for splitting a spectrum of the intermediate frequency centered real signal (440) into spectra of intermediate frequency modulated in-phase and quadrature signals (434, 438);

30 - means for down-shifting spectra of the intermediate frequency modulated in-phase and quadrature signals (434, 438), the shift down in frequencies of the spectra inserting zero frequency into the center of the frequency difference of the spectra;

- means for compressing downshifted spectra of the intermediate frequency modulated in-phase and quadrature signals (432, 436), the frequency difference between the compressed downshifted spectra being at most half the frequency difference of the spectra.

5 12. A circuit (400) according to claim 11, wherein the means for splitting the spectrum of the intermediate frequency centered real signal (440) comprise a de-multiplexer (439) for de-multiplexing the real signal (440) to an in-phase branch of the in-phase and quadrature signals (434) and a quadrature branch of the in-phase and quadrature signals (438).

10

13. A circuit (400) according to claim 11 or 12, wherein the means for downshifting spectra of the intermediate frequency modulated in-phase and quadrature signals (434, 438) comprise:

15 - a first down-converting element (433) for frequency down-converting an in-phase branch of the in-phase and quadrature signals (434);
- a second down-converting element (437) for frequency down converting a quadrature branch of the in-phase and quadrature signals (438).

14. A circuit (400) according to at least one of the claims 11 to 13, wherein the 20 means for compressing downshifted spectra of intermediate frequency modulated in-phase and quadrature signals (432, 436) comprise:

25 - a first decimation processor (431) for decimating a down-converted in-phase branch of the in-phase and quadrature signals (432) by at least one;
- a second decimation processor (435) for decimating a down-converted quadrature branch of the in-phase and quadrature signals (436) by at least one;
- a first decimation filter (431) for filtering a decimated down-converted in-phase branch of the in-phase and quadrature signals;
- a second decimation filter (435) for filtering a decimated down-converted quadrature branch of the in-phase and quadrature signals;
30 - a third decimation processor (414) for decimating a filtered decimated down-converted in-phase branch of the in-phase and quadrature signals (415) by at least one;
- a fourth decimation processor (424) for decimating a filtered decimated down-converted quadrature branch of the in-phase and quadrature signals (425) by at least one;

- a third decimation filter (412) for filtering a filtered double decimated down-converted in-phase branch of the in-phase and quadrature signals (413);
- a fourth decimation filter (422) for filtering a filtered double decimated down-converted quadrature branch of the in-phase and quadrature signals (423).

5

15 A circuit (400) according to at least one of the claims 12 to 14, wherein at least one of the decimation filters (412, 422, 431, 435) is a low pass filter.

16. A circuit (400) according to claim 15, wherein at least one of the low pass
10 filters (412, 422, 431, 435) is a half band filter.

17. A circuit (400) according to at least one of the claims 12 to 16, wherein the circuit (400) is adapted for decimating the in-phase and quadrature signals (434, 438) by four.

15 18. A circuit (400) according to claim 17, wherein

- the first decimation processor (431) is adapted for decimating the down-converted in-phase branch of the in-phase and quadrature signals (432) by two;
- the second decimation processor (435) is adapted for decimating the down-converted quadrature branch of the in-phase and quadrature signals (436) by two;
- the third decimation processor (414) is adapted for decimating the filtered decimated down-converted in-phase branch of the in-phase and quadrature signals (415) by two;
- the fourth decimation processor (424) is adapted for decimating the filtered decimated down-converted quadrature branch of the in-phase and quadrature signals (425) by two.

20

19. A circuit (400) according to at least one of the claims 12 to 18, wherein

- the first decimation processor (431) and the first decimation filter (431) and the first down-converting element (433) and the second decimation processor (435) and the second decimation filter (435) and the second down-converting element (437) and the de-multiplexer (439) is a poly phase implementation of a real to quadrature converter;
- the third decimation processor (414) and the third decimation filter (412) is a poly phase implementation of a decimate by two half band filter;

- the fourth decimation processor (424) and the fourth decimation filter (422) is a poly phase implementation of a decimate by two half band filter.

20. A circuit (400) according to claim 19, wherein

5 - the first down-converting element (433) is implemented as a multiplexer adapted for multiplexing between a true and a negated value of the in-phase branch of the in-phase and quadrature signals (434);

- the second down-converting element (437) is implemented as a multiplexer adapted for multiplexing between a true and a negated value of the quadrature branch of the 10 in-phase and quadrature signals (438).

21. A method (100) for converting base-band modulated in-phase and quadrature signals (111, 121) to an intermediate frequency centered real signal (140), characterized in that the method (100) comprises the steps of:

15 - dispersing spectra of the base band modulated in-phase and quadrature signals (111, 121), the frequency difference between the dispersed spectra being at least twice the frequency difference of the spectra;

- up-shifting dispersed spectra of base band modulated in-phase and quadrature signals (132, 136), the shift up in frequencies of the dispersed spectra omitting at 20 least zero frequency from the substantial part of the spectra;

- mirroring up-shifted dispersed spectra of base band modulated in-phase and quadrature signals (134, 138) into a spectrum of the intermediate frequency centered real signal (140).

25 22. A method (100) according to claim 21, wherein dispersing spectra of the base band modulated in-phase and quadrature signals (111, 121) comprises the steps of:

- a first interpolation process (112) interpolating an in-phase branch of the in-phase and quadrature signals (111) by at least one;

- a second interpolation process (122) interpolating a quadrature branch of the 30 in-phase and quadrature signals (121) by at least one;

- a first interpolation filter process (114) filtering an interpolated in-phase branch of the in-phase and quadrature signals (113);

- a second interpolation filter process (124) filtering an interpolated quadrature branch of the in-phase and quadrature signals (123);

- a third interpolation process (131) interpolating a filtered interpolated in-phase branch of the in-phase and quadrature signals (115) by at least one;
- a fourth interpolation process (135) interpolating a filtered interpolated quadrature branch of the in-phase and quadrature signals (125) by at least one;

5 - a third interpolation filter process (131) filtering a filtered double interpolated in-phase branch of the in-phase and quadrature signals;

 - a fourth interpolation filter process (135) filtering a filtered double interpolated quadrature branch of the in-phase and quadrature signals.

10 23. A method (100) according to claim 21 or 22, wherein up shifting dispersed spectra of the base band modulated in-phase and quadrature signals (132, 136) comprises the steps of:

- a first up-converting process (133) for frequency up-converting a double filtered double interpolated in-phase branch of the in-phase and quadrature signals (132);

15 - a second up-converting process (137) for frequency up converting a double filtered double interpolated quadrature branch of the in-phase and quadrature signals (136).

24. A method (100) according to at least one of the claims 21 to 23, wherein mirroring up-shifted dispersed spectra of the base band modulated in-phase and quadrature signals (134, 138) comprises a multiplexing process (139) multiplexing an up-converted double filtered double interpolated in-phase branch of the in-phase and quadrature signals (134) and an up-converted double filtered double interpolated quadrature branch of the in-phase and quadrature signals (138) to a real signal (140).

25 25. A method (100) according to at least one of the claims 22 to 24, wherein at least one of the interpolation filter processes (114, 124, 131, 135) is a low pass filter process.

26. A method (100) according to claim 25, wherein at least one of the low pass filter processes (114, 124, 131, 135) is a half band filter process.

30 27. A method (100) according to at least one of the claims 22 to 26, wherein the method (100) is adapted for interpolating the in-phase and quadrature signals (111, 121) by four.

28. A method (100) according to claim 27, wherein

- the first interpolation process (112) is adapted for interpolating the in-phase branch of the in-phase and quadrature signals (111) by two;
- the second interpolation process (122) is adapted for interpolating the quadrature branch of the in-phase and quadrature signals (121) by two;
- 5 - the third interpolation process (131) is adapted for interpolating the filtered interpolated in-phase branch of the in-phase and quadrature signals (115) by two;
- the fourth interpolation process (135) is adapted for interpolating the filtered interpolated quadrature branch of the in-phase and quadrature signals (125) by two.

10 29. A method (100) according to at least one of the claims 22 to 28, wherein

- the first interpolation process (112) and the first interpolation filter process (114) is a poly phase implementation of an interpolate by two half band filter process;
- the second interpolation process (122) and the second interpolation filter process (124) is a poly phase implementation of an interpolate by two half band filter process;
- the third interpolation process (131) and the third interpolation filter process (131) and the first up-converting process (133) and the fourth interpolation process (135) and the fourth interpolation filter process (135) and the second up-converting process (137) and
- 15 20 the multiplexing process (139) is a poly phase implementation of a quadrature to real converting process.

30. A method (100) according to claim 29, wherein

- the first up-converting process (133) is implemented as a multiplexing process adapted for multiplexing between a true and a negated value of the double filtered double interpolated in-phase branch of the in-phase and quadrature signals (132);
- the second up-converting process (137) is implemented as a multiplexing process adapted for multiplexing between a true and a negated value of the double filtered double interpolated quadrature branch of the in-phase and quadrature signals (136).

30 31. A method (400) for converting an intermediate frequency centered real signal (440) to base-band modulated in-phase and quadrature signals (411, 421), characterized in that the method (400) comprises the steps of:

- splitting a spectrum of the intermediate frequency centered real signal (440) into spectra of intermediate frequency modulated in-phase and quadrature signals (434, 438);
 - down-shifting spectra of the intermediate frequency modulated in-phase and quadrature signals (434, 438), the shift down in frequencies of the spectra inserting zero frequency into the center of the frequency difference of the spectra;
 - compressing downshifted spectra of the intermediate frequency modulated in-phase and quadrature signals (432, 436), the frequency difference between the compressed downshifted spectra being at most half the frequency difference of the spectra.

10 32. A method (400) according to claim 31, wherein splitting the spectrum of the intermediate frequency centered real signal (440) comprises a de-multiplexing process (439) de-multiplexing the real signal (440) to an in-phase branch of the in-phase and quadrature signals (434) and a quadrature branch of the in-phase and quadrature signals (438).

15 33. A method (400) according to claim 31 or 32, wherein down-shifting spectra of the intermediate frequency modulated in-phase and quadrature signals (434, 438) comprises the steps of:

- a first down-converting process (433) for frequency down-converting an in-phase branch of the in-phase and quadrature signals (434);
- a second down-converting process (437) for frequency down converting a quadrature branch of the in-phase and quadrature signals (438).

20 34. A method (400) according to at least one of the claims 31 to 33, wherein compressing down-shifted spectra of intermediate frequency modulated in-phase and quadrature signals (432, 436) comprises the steps of:

- a first decimation process (431) decimating a down-converted in-phase branch of the in-phase and quadrature signals (432) by at least one;
- a second decimation process (435) decimating a down-converted quadrature branch of the in-phase and quadrature signals (436) by at least one;

25 30 - a first decimation filter process (431) filtering a decimated down-converted in-phase branch of the in-phase and quadrature signals;

30 - a second decimation filter process (435) filtering a decimated down-converted quadrature branch of the in-phase and quadrature signals;

- a third decimation process (414) decimating a filtered decimated down-converted in-phase branch of the in-phase and quadrature signals (415) by at least one;
- a fourth decimation process (424) decimating a filtered decimated down-converted quadrature branch of the in-phase and quadrature signals (425) by at least one;

5 - a third decimation filter process (412) filtering a filtered double decimated down-converted in-phase branch of the in-phase and quadrature signals (413);

 - a fourth decimation filter process (422) filtering a filtered double decimated down-converted quadrature branch of the in-phase and quadrature signals (423).

10 35. A method (400) according to at least one of the claims 32 to 34, wherein at least one of the decimation filter processes (412, 422, 431, 435) is a low pass filter process.

 36. A method (400) according to claim 35, wherein at least one of the low pass filter processes (412, 422, 431, 435) is a half band filter process.

15 37. A method (400) according to at least one of the claims 32 to 36, wherein the method (400) is adapted for decimating the in-phase and quadrature signals (434, 438) by four.

20 38. A method (400) according to claim 37, wherein

- the first decimation process (431) is adapted for decimating the down-converted in-phase branch of the in-phase and quadrature signals (432) by two;
- the second decimation process (435) is adapted for decimating the down-converted quadrature branch of the in-phase and quadrature signals (436) by two;

25 - the third decimation process (414) is adapted for decimating the filtered decimated down-converted in-phase branch of the in-phase and quadrature signals (415) by two;

 - the fourth decimation process (424) is adapted for decimating the filtered decimated down-converted quadrature branch of the in-phase and quadrature signals (425) by two;

30 39. A method (400) according to at least one of the claims 32 to 38, wherein

- the first decimation process (431) and the first decimation filter process (431) and the first down-converting process (433) and the second decimation process (435) and the second decimation filter process (435) and the second down-converting process (437) and the de-multiplexing process (439) is a poly phase implementation of a real to quadrature converting process;
- 5
 - the third decimation process (414) and the third decimation filter process (412) is a poly phase implementation of a decimate by two half band filter process;
 - the fourth decimation process (424) and the fourth decimation filter process (422) is a poly phase implementation of a decimate by two half band filter process.
- 10
 - 40. A method (400) according to claim 39, wherein
 - the first down-converting process (433) is implemented as a multiplexing process adapted for multiplexing between a true and a negated value of the in-phase branch of the in-phase and quadrature signals (434);
 - the second down-converting process (437) is implemented as a multiplexing process adapted for multiplexing between a true and a negated value of the quadrature branch of the in-phase and quadrature signals (438).
- 15
 - 41 An apparatus comprising a first circuit (100) for performing any of the methods defined in claims 1 through 10 and a second circuit (400) for performing any of the methods defined in claims 11 through 20.
- 20
 - 42. A computer readable medium having stored thereon instructions for causing one or more processing units to execute the methods according to any of the claims 21 through 30.
- 25
 - 43. A computer readable medium having stored thereon instructions for causing one or more processing units to execute the methods according to any of the claims 31 through 40.

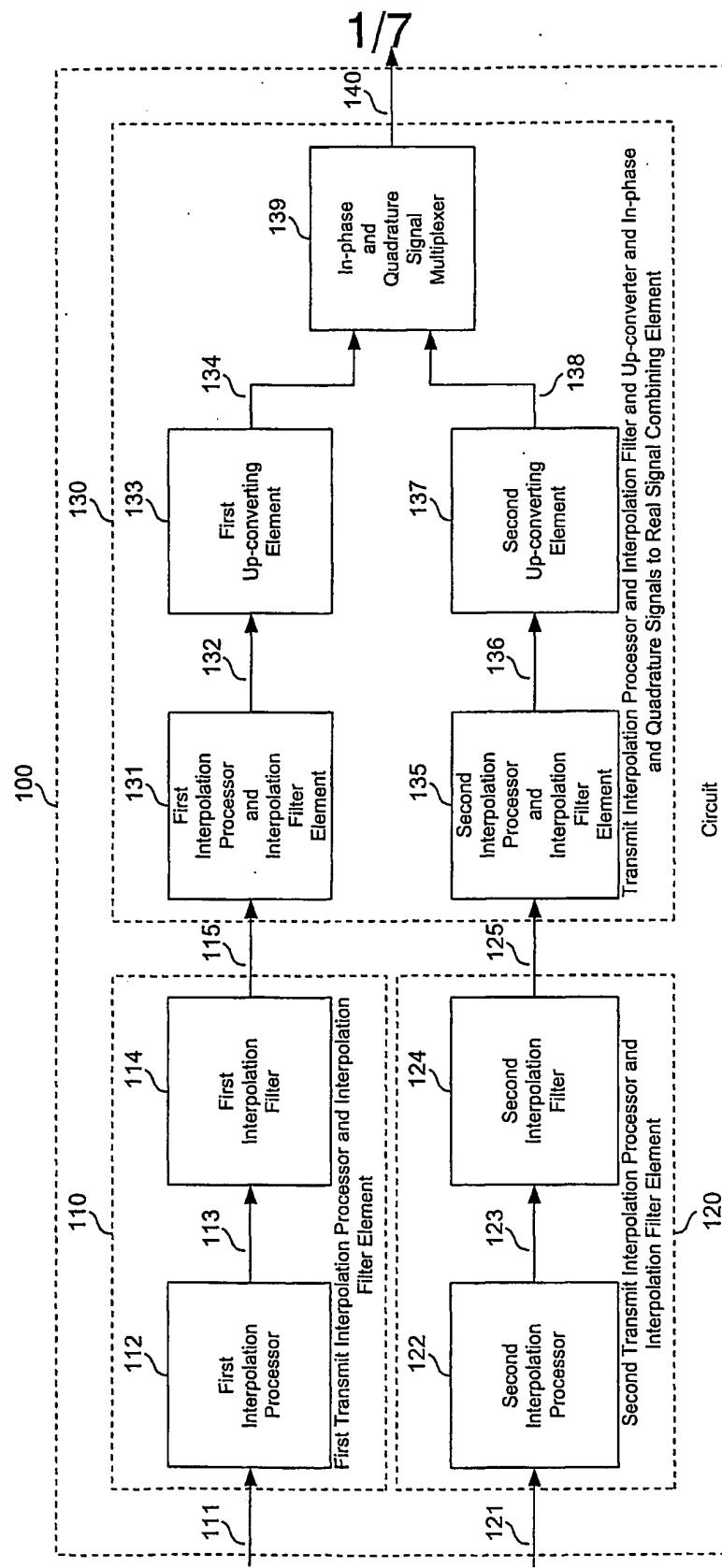


FIG. 1

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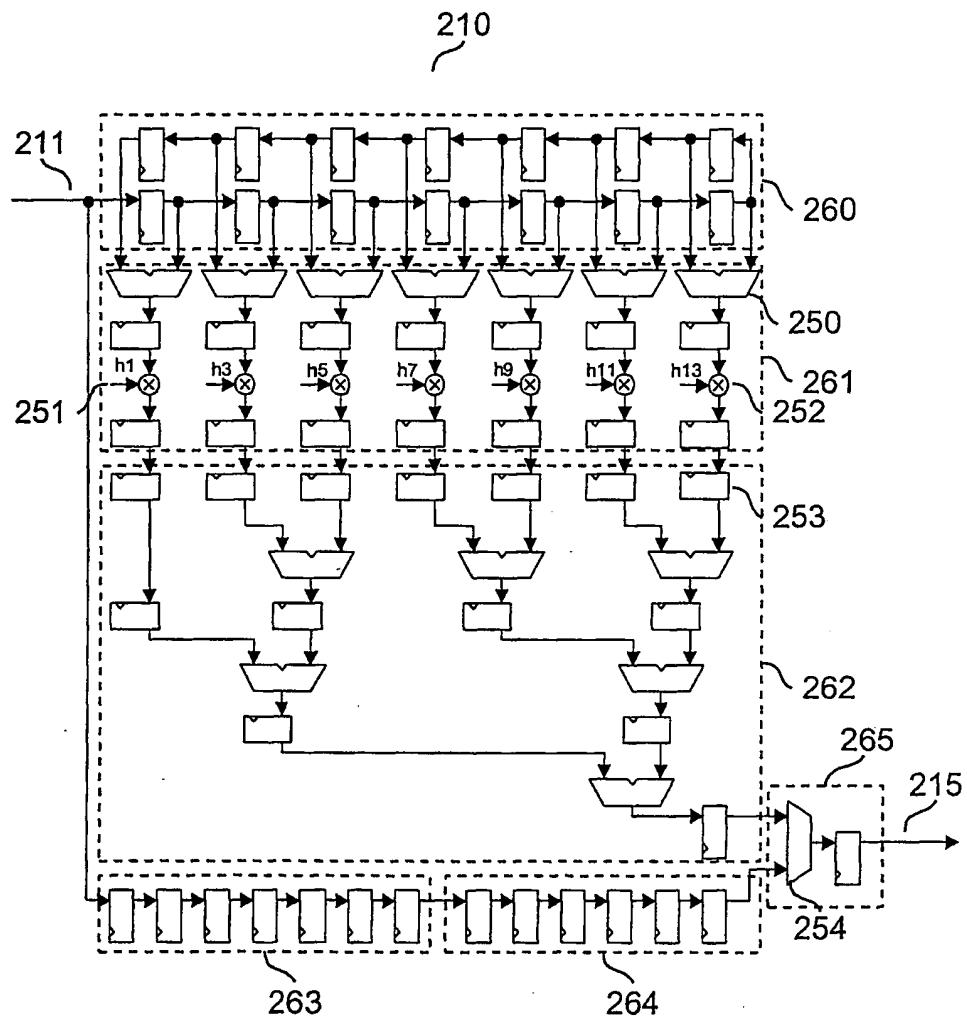


FIG.2

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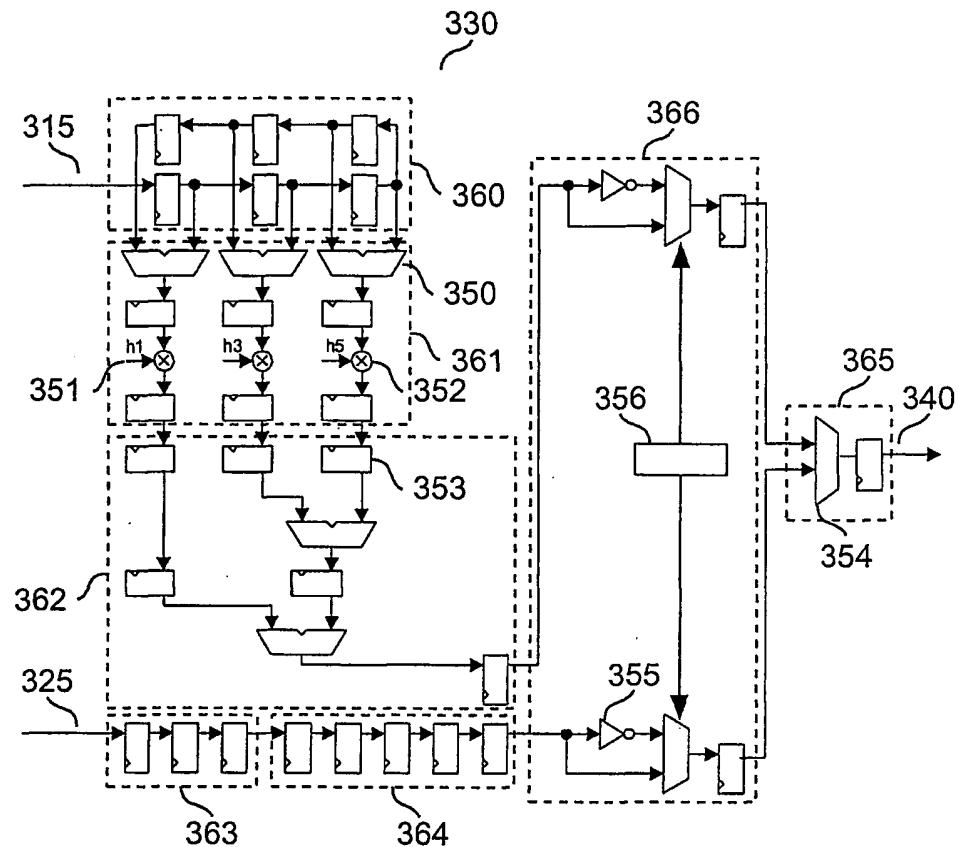


FIG.3

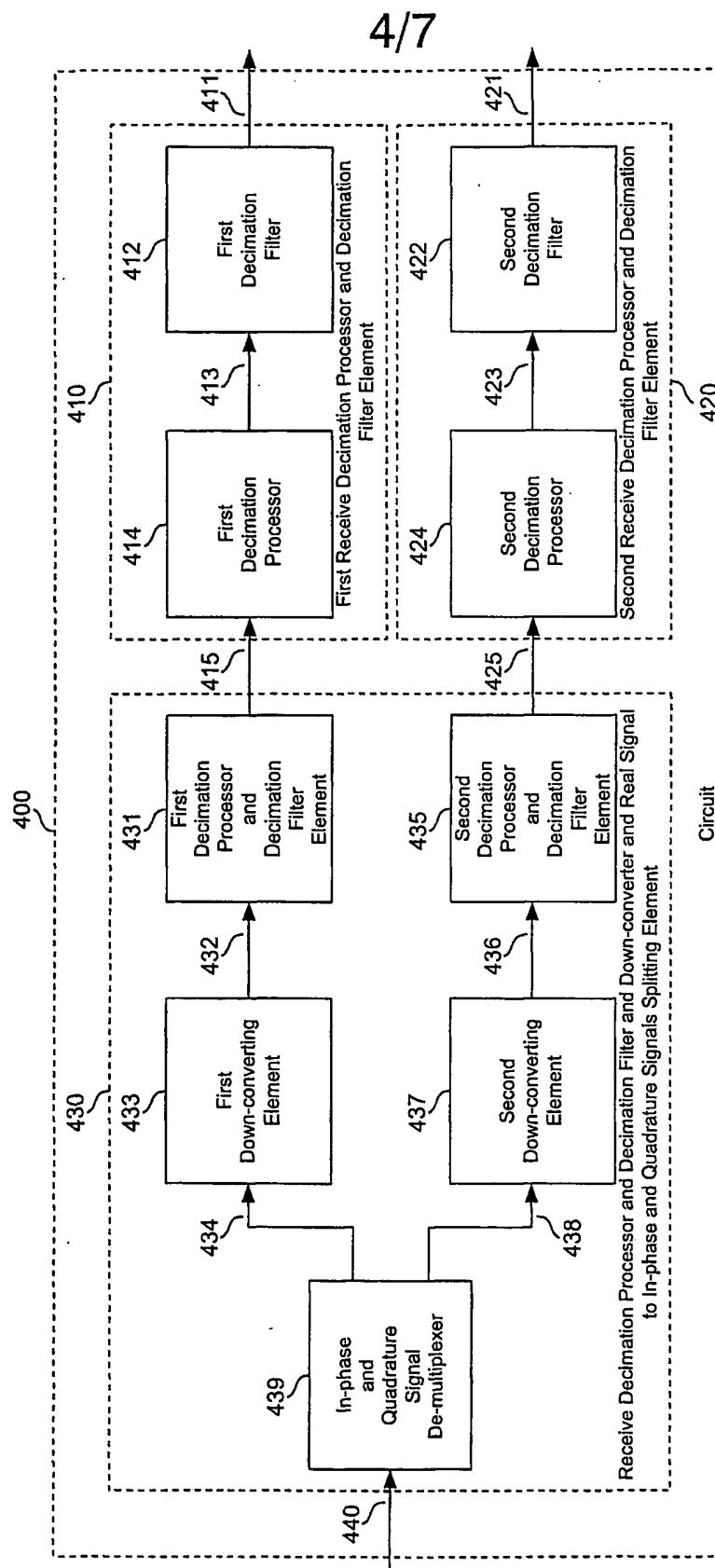


FIG. 4

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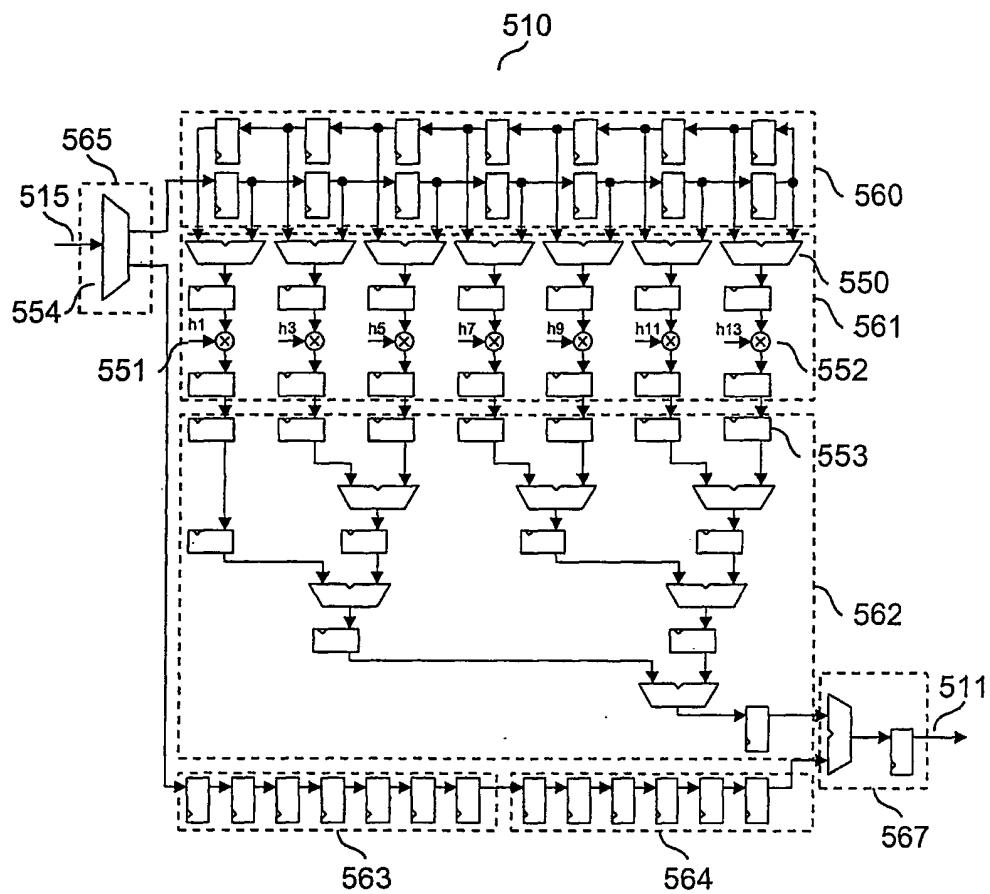


FIG.5

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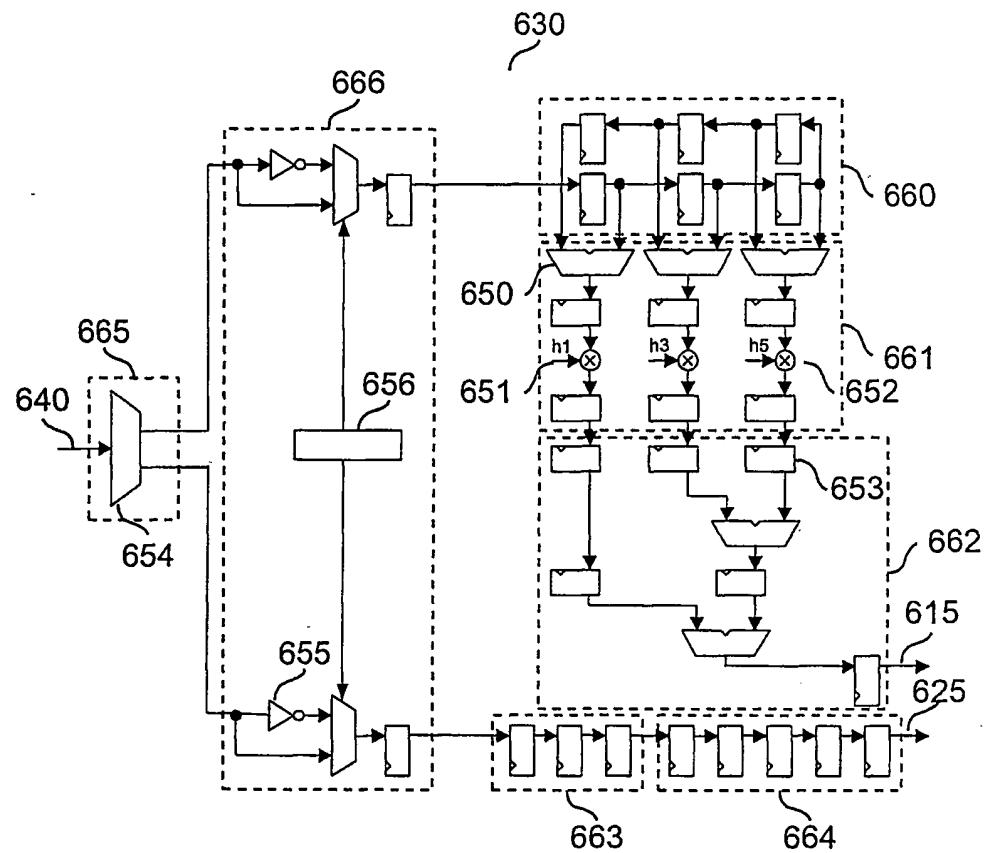


FIG.6

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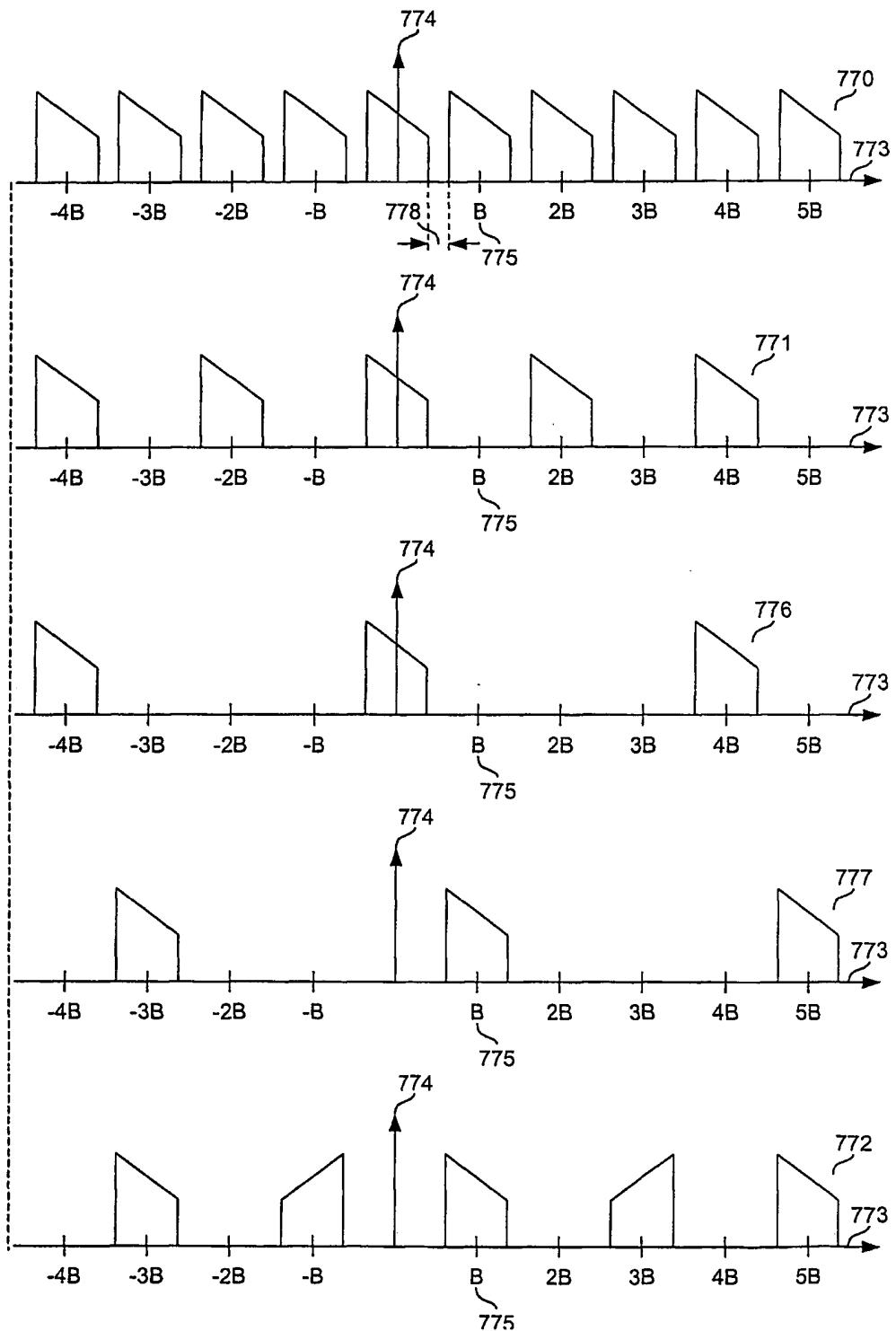


FIG.7

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